AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph 0007 with the following:

[0007] Accordingly, the present invention is a system for synchronous sampling of analog signal inputs for a plurality of electronic instruments, using an encoded time signal, comprising: an externally generated encoded time signal provided to the plurality of electronic instruments suitable for insuring accurate time-of-day clock synchronization for the electronic instruments; an edge detector responsive to the encoded time signal to produce a series of pulses based on the edges of the encoded time signal; and a phase-locked ~~phrase-locked~~ loop assembly producing an output sampling synchronization signal which is phase-locked ~~phrase-locked~~ to said pulses at the output of the edge detector, such that the output sampling synchronization signal occurs at the beginning of each predetermined time period with successive synchronization signals being evenly spaced in the interval between the beginning of each successive predetermined time, for synchronization of data sampling in said plurality of instruments.

Please replace paragraph 0016 with the following:

[0016] In FIG. 2, the complete IRIG-B transmission identifying one particular second in a year is shown at 17. The encoding for seconds is designated at 18, minutes at 22, hours at 26, 0-99 days at 30, and hundreds of days at 32. The particular second identified is the 34th ~~35th~~ second, of the 12th minute, of the 17th hour, of the 209th day. An "R" field 34, comprising two successive "P" bits, separates successive frames. In the present invention, the IRIG-B encoded time signal or other encoded time signal is also used for its conventional time-of-day clock synchronization of a plurality of devices. However, it is also used to produce a data sampling (or other function) synchronization signal for the same devices.

Please replace paragraph 0018 with the following:

[0018] Referring again to FIG. 1, the time between successive edges of the IRIG-B signal could be 2, 5 or 8 milliseconds, based on a 10-millisecond bit. Thus, the output of the edge detector 40 will be a series of pulses, separated by 2, 5 or 8 milliseconds. Each edge will be a multiple of 1 kHz away from the last edge. The output of the edge detector 40 is applied to a phase-locked-loop 42 which is arranged to produce an output signal of selected frequency, 8 kHz in the embodiment shown, phase-locked to the pulses from the edge detector. Since the transitions of

the output signal from the phase-locked-loop occur simultaneously with transitions in the IRIG-B signal input, a data sampling synchronization signal occurs precisely at the beginning of each second, as defined by the IRIG-B input signal, in particular, the rising edge of the second "P" bit in the "R" field 34 ~~32~~. The 8 kHz output signal on line 47 is the data sampling synchronization signal for the plurality of synchronized devices.

Please replace paragraph 0020 with the following:

[0020] The output of the filter controls a numerically controlled counter (NCO) 46, which is designed to produce an output signal (line 47) of selected frequency, i.e. 8 kHz in this particular embodiment. It could, however, be other integral multiples of 1 kHz, including 1 kHz, 2 kHz, 3 kHz, etc. The NCO in operation counts nominally to the output frequency, which in the embodiment shown is 8 kHz. The count is adjusted by the output of the filter (+/-); the adjustment allows the system to lock to the incoming signal. The output of counter 46 is applied to the feedback circuit 50 for the phase-locked-loop. The feedback circuit 50 converts the 8 kHz signal to a 1 kHz signal, which is then applied to the phase detector 43 ~~42~~ for comparison with the signal from the edge detector.